FAST HIGH VOLTAGE TRANSISTOR SWITCHES

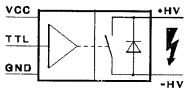
DESCRIPTION

The solid-state switches of the HTS-UF (Ultra Fast) series have been specially designed for high voltage pulse generators with a short pulse duration and extreme edge steepness. The HTS-UF switches are distinguished above all by a rise time which remains widely constant over a large range of operating voltages and loads. For low voltage operation a special stage tapping option is available which allows fast switching also in the hundred volt range. In contrast to conventional high voltage switches, e.g. with cold cathode tubes, the transistor switches of the HTS-UF series have a very low jitter and the lifetime typical of semi-conductor devices. At the input side all that is needed is a TTL-compatible control signal and a 5-volt auxiliary voltage. The internal driving circuit takes care of signal conditioning, auxiliary voltage monitoring, frequency limitation and temperature protection. The switches are triggered by a positive going pulse of 2 to 10 volts amplitude. The on-time after being triggered is typically 200 nanoseconds for standard devices. On-time values of between 5 ns and 1 μs are optionally available (Please refer to data table). Extremely short pulses of a few nanoseconds may simply be generated by means of a single switch with short on-time option and a low working resistance (see Fig. 3). The recovery time after a switching cycle is less than 1 μs, making burst frequencies of more than 1 MHz possible. The galvanic isolation allows high-side switching in both polarities.

CIRCUIT DESIGN RECOMMENDATIONS

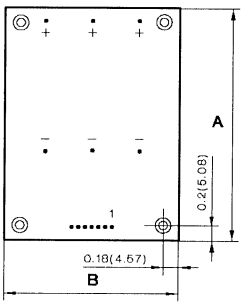
Because of the extremely rapid rates of voltage and current change, all leads and circuit paths should be kept as short and as wide as possible. Part components such as R_L, R_S, C_{BP} and C_B must be low-inductance types and should be placed as near as possible to the switch, preferably right below the module on the surface of the soldering side. Ground conducting tracks must be connected as short as possible to a common ground point. Induction loop areas of dynamically current-carrying circuit paths should be kept as small as possible as well as the circuit paths of the control side should not be formed as induction loops. To achieve shortest transition times and clear pulse shapes the application of stripline techniques is recommended. In the interest of a good noise immunity the logic ground must be connected with the ground of the high voltage side. This galvanic linkage can be replaced by a ceramic capacitor of 1 to 10 nF for "floating" high- voltage circuits. Three pins in the middle of the unit are used as HV minus pole and the outer three pins as HV plus pole of switch. All pins of each pole should be connected together to obtain a low terminal stray inductance. The control input wiring must be kept on distance to the HV wiring. Long leads to trigger input (Pin 1) should be shielded and terminated properly. A decoupling capacitor of roughly 10 μF between pin 3 (5 VDC input) and pin 4 (5 VDC return) is recommended for low jitter. In addition the jitter can be minimized by use of trigger sources with

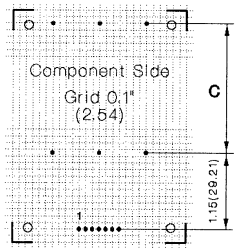
HTS 50-08-UF	5000 VDC / 80 Amps
HTS 50-12-UF	5000 VDC / 120 Amps
HTS 80-12-UF	8000 VDC / 120 Amps
HTS 80-20-UF	8000 VDC / 200 Amps



-Patented-

ULTRA FAST
Fixed On-Time

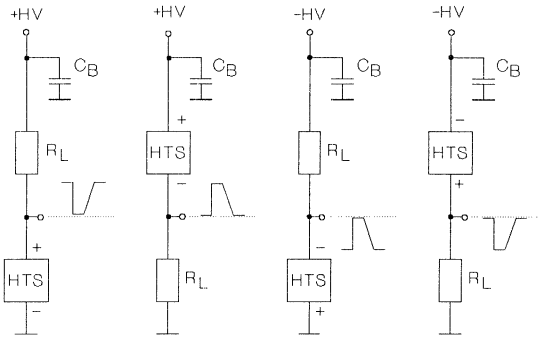




Attachment: Metric srews, 3 mm dia.
Dimensions in inches and (millimeters)

Model	A	B	C
50-08-UF 50-12-UF	3.5 (89)	2.52 (64)	2.06(52.07)
80-12-UF	4.8 (122)	2.52 (64)	3.36(85.09)
80-20-UF	4.8 (122)	3.5 (89)	3.36(85.09)

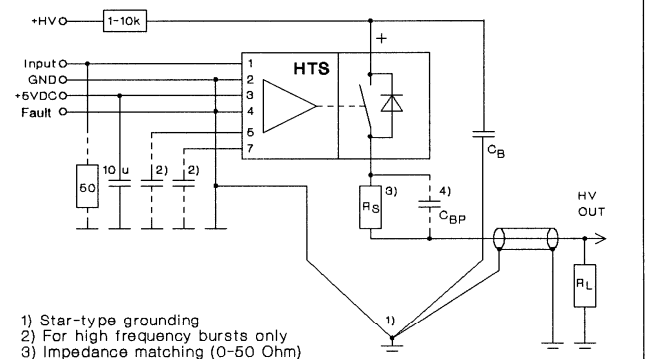
Basic Circuits

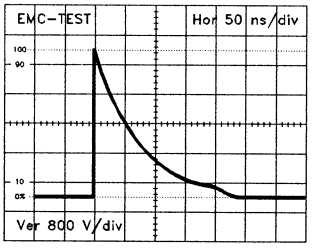


>3 volt amplitude and ripple-free auxiliary power supplies. In applications with high-frequency bursts it is necessary to buffer two internally generated driver voltages (22 VDC and 400 VDC) by means of external capacitors insofar as more than 10 pulses per pulse train are generated in less than 20 μs. In such a case the 22 VDC output (pin 5) and the 400 VDC output (pin 7) are connected to suitable electrolyte capacitors.

For further design recommendations please refer to the instructions.

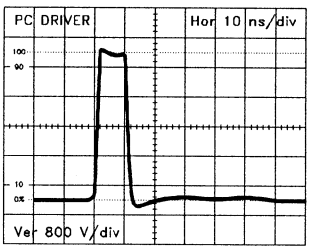
Connection





EMC Burst Tester according to IEC 801-4 using HTS 80-12-UF

Load resistor R_L:	50 Ohm
Series resistor R_S:	27 Ohm
Bypass cap. C_{BP}:	None
Energy storage C_B:	820 pF
Input voltage:	8000 VDC
Pulse amplitude:	4000 VDC
Pulse width (50%):	50 ns
Rise time 10-90%:	2.0 ns



10 ns Pulse Generator / Pockels Cell Driver using HTS 80-12-UF + Option 02

Load resistor R_L:	50 Ohm
Series resistor R_S:	15 Ohm
Bypass cap. C_{BP}:	56 pF
Energy storage C_B:	22 nF
Input voltage:	8000 VDC
Pulse amplitude:	4000 VDC
Pulse width (50%):	10 ns
Rise time 10-90%:	2.2 ns

TECHNICAL DATA

SPECIFICATION	SYMB.	CONDITION / COMMENT		50-08-UF	50-12-UF	80-12-UF	80-20-UF	UNIT
Max. Operating Voltage	$V_{O(max)}$	I_{off} < 100 µADC		5000	5000	8000	8000	VDC
Lowest Useful Operating	$V_{O(min)}$	Standard devices		500	500	800	800	
Voltage (cf. option 05)		Dito with option 01/02/03		1200	1200	2000	2000	VDC
Typical Breakdown Voltage	V_{Br}	I_{off} > 1 mADC, T_{case} = 70°C		5500	5500	8800	8800	VDC
Galvanic Isolation	V_I	HV side against control side		>10000				VDC
Maximum Peak Current	$I_{P(max)}$	t_p < 50 ns		80	120	120	200	ADC
Current Change Rate	di/dt	Optimized PCB design		55	60	50	50	A/ns
Static On-Resistance	R_{stat}	Current-dependent	0.1x$I_{P(max)}$	4	2.8	4.5	2.7	
			@ $I_{P(max)}$	10	7	11.3	6.8	Ω
Max. Off-State Current	I_{off}	0.8 x V_O		50	55	55	70	µADC
Turn-On Delay Time	$t_{d(on)}$	@ $I_{P(max)}$		60	60	60	70	ns
Turn-On Rise Time	$t_{r(on)}$	0.8 x V_O, 0.8 x $I_{P(max)}$		1.2	1.6	2.0	3.1	ns
On-Time (Standard)	t_{on}	Voltage-dependent	@ $V_{O(max)}$	200	200	200	150	
			@ $V_{O(min)}$	400	400	400	300	ns
Minimum Optional On-Time	$t_{on(min)}$	+25% tolerance at $V_{O(max)}$		5	10	10	20	ns
Maximum Optional On-Time	$t_{on(max)}$	Voltage-dependent tolerance		1				µs
Switch Recovery Time	t_{rc}	(Minimum pulse spacing)		1				µs
Typical Turn-On Jitter	$t_{j(on)}$	V_{aux} / V_{tr} = 5.0 VDC		100				ps
Max. Switching Frequency	$f_{(max)}$	Continuously, @ $V_{O(max)}$		3	2	2	2	kHz
Max. Power Dissipation	$P_{d(max)}$	T_{case} = 25°C, cf. option 07		10	10	15	20	Watts
Linear Derating		Above 25 °C		0.22	0.22	0.33	0.44	W/K
Temperature Range	T_O	Extented range on request		-40...70				°C
Natural Capacitance	C_N	@ $V_{O(max)}$		105	160	100	170	pF
Coupling Capacitance	C_C	HV side against control side		10	11	17	18	pF
Diode Reverse Recovery	t_{rrc}	0.2 x $I_{P(max)}$		1				µs
Auxiliary Supply Voltage	V_{aux}	Stabilized to ± 5%		5.0				VDC
Auxiliary Supply Current	I_{aux}	@ $f_{(max)}$		400				mADC
Trigger Signal Voltage	V_{tr}	> 3VDC recommended		2-10				VDC
Dimensions		20 mm height on request		89x64x31	89x64x31	122x64x31	122x89x31	mm³
Weight				480	500	650	900	g

ORDERING INFORMATION:

HTS 50-08-UF	Transistor switch, 5000 VDC, 80 Amps.
HTS 50-12-UF	Transistor switch, 5000 VDC, 120 Amps.
HTS 80-12-UF	Transistor switch, 8000 VDC, 120 Amps.
HTS 80-20-UF	Transistor switch, 8000 VDC, 200 Amps.
Option 01	On-time 5ns. See $t_{on(min)}$ specifications!
Option 02	On-time 10ns. See $t_{on(min)}$ specifications!
Option 03	On-time 20ns
Option 04	Customized on-time. Values between $t_{on(min)}$ and $t_{on(max)}$.
Option 05	Stage tapping for alternative operation at low voltages. One or more tappings are possible in steps of 500 VDC. Please specify the required tapping voltage with order.
Option 06	Flame retardend casting resin according to UL 94-VO.
Option 07	Metal case for an increased $P_{d(max)}$ of up to 1500 Watts and accordingly increased $f_{(max)}$. Available from II/94.

All data and specifications subject to change without notice. Custom designed devices on request.